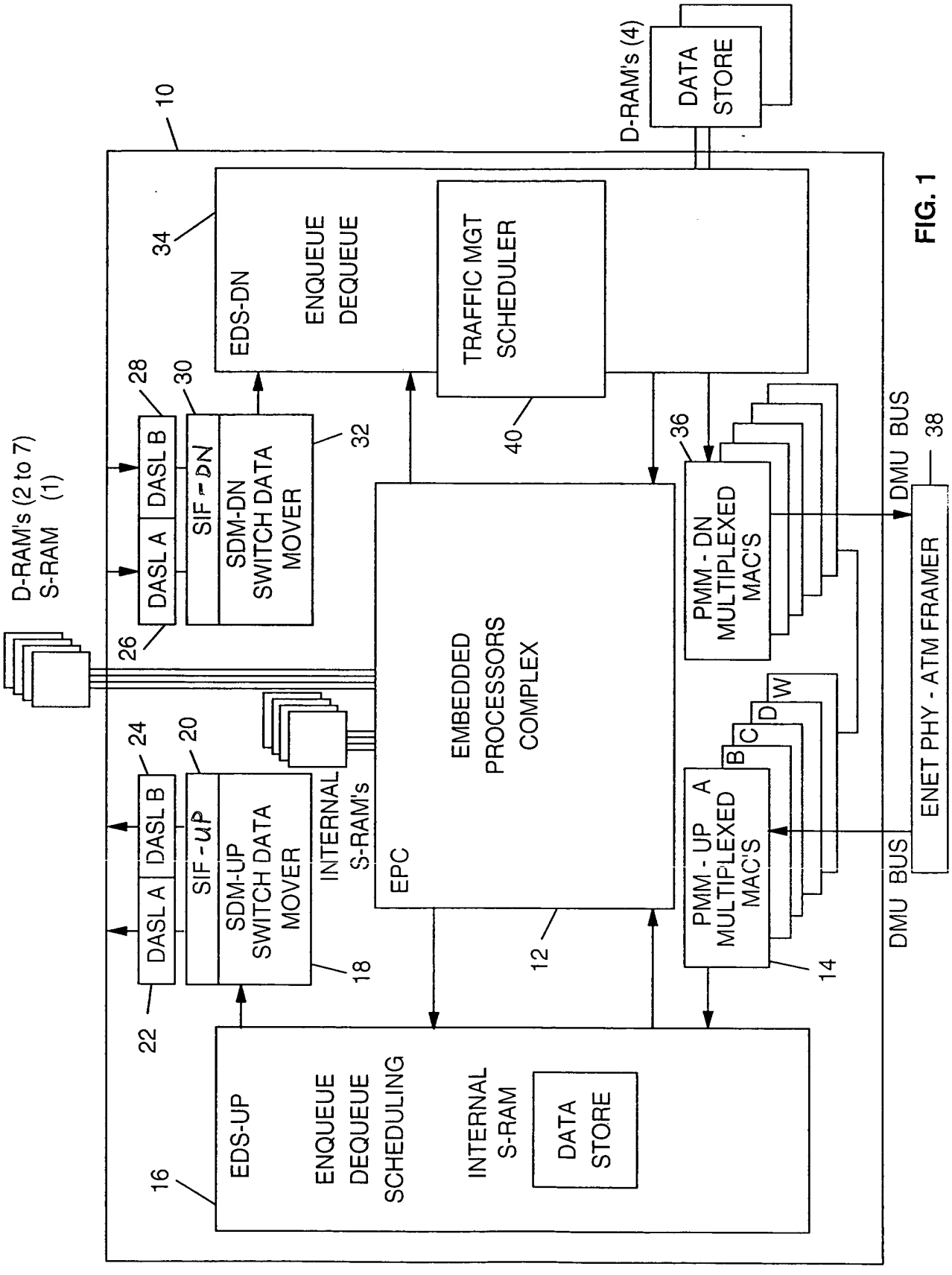
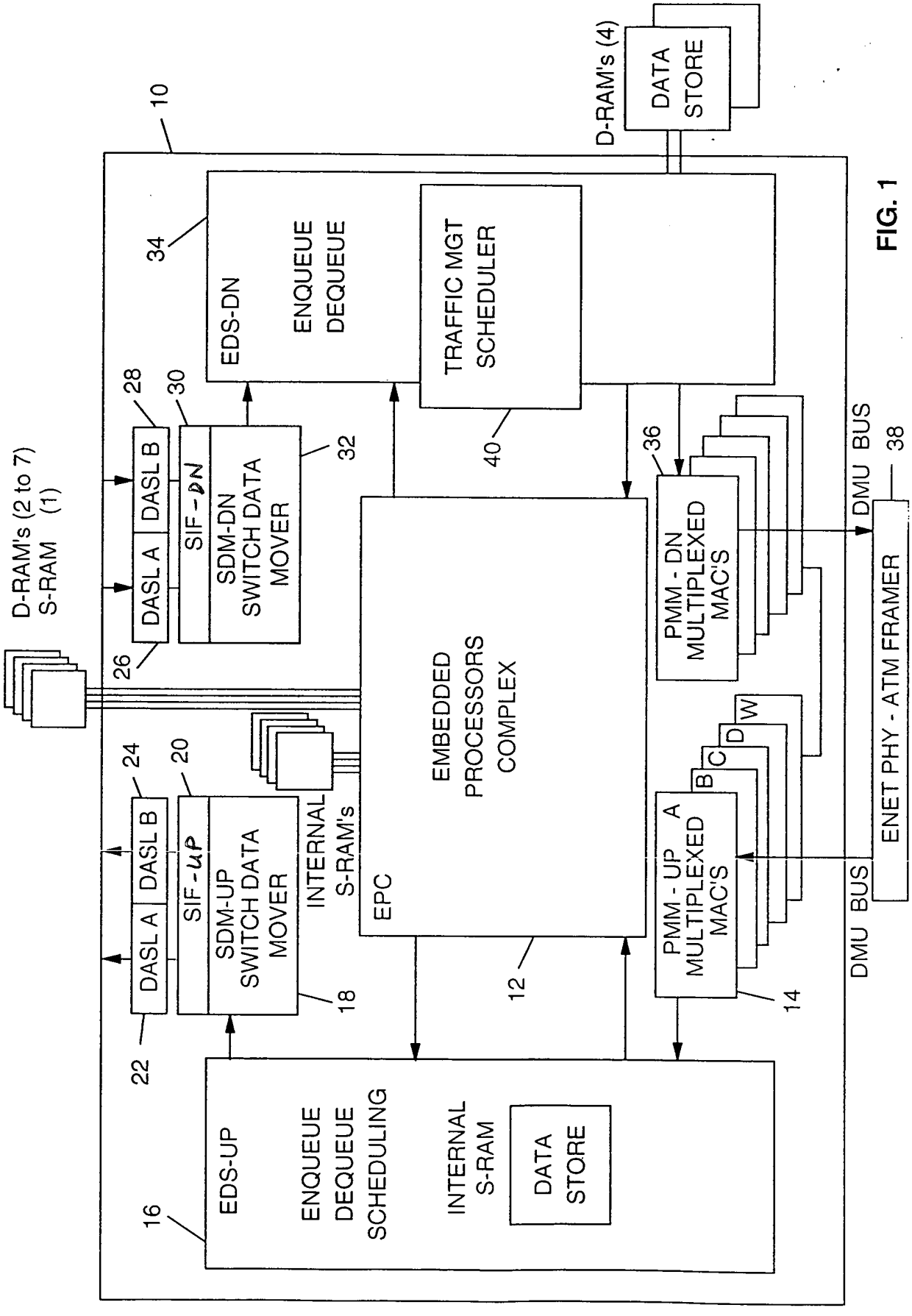

10
D-RAM's (4)
DATA STORE
34
EDS-DN
ENQUEUE
DEQUEUE
TRAFFIC MGT SCHEDULER
40
28
30
DASL B
DASL A
SIF - DN
SDM-DN SWITCH DATA MOVER
32
36
PMM - DN MULTIPLEXED MAC'S
DMU BUS
38
D-RAM's (2 to 7)
S-RAM (1)
26
EMBEDDED PROCESSORS COMPLEX
INTERNAL S-RAM's
EPC
12
24
20
DASL B
DASL A
SIF - UP
SDM-UP SWITCH DATA MOVER
18
PMM - UP A MULTIPLEXED MAC'S
B
C
D
W
14
DMU BUS
ENET PHY - ATM FRAMER
22
16
EDS-UP
ENQUEUE
DEQUEUE
SCHEDULING
INTERNAL S-RAM
DATA STORE

FIG. 1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EDS-UP
ENQUEUE
DEQUEUE
SCHEDULING
INTERNAL S-RAM
DATA STORE

FIG. 1

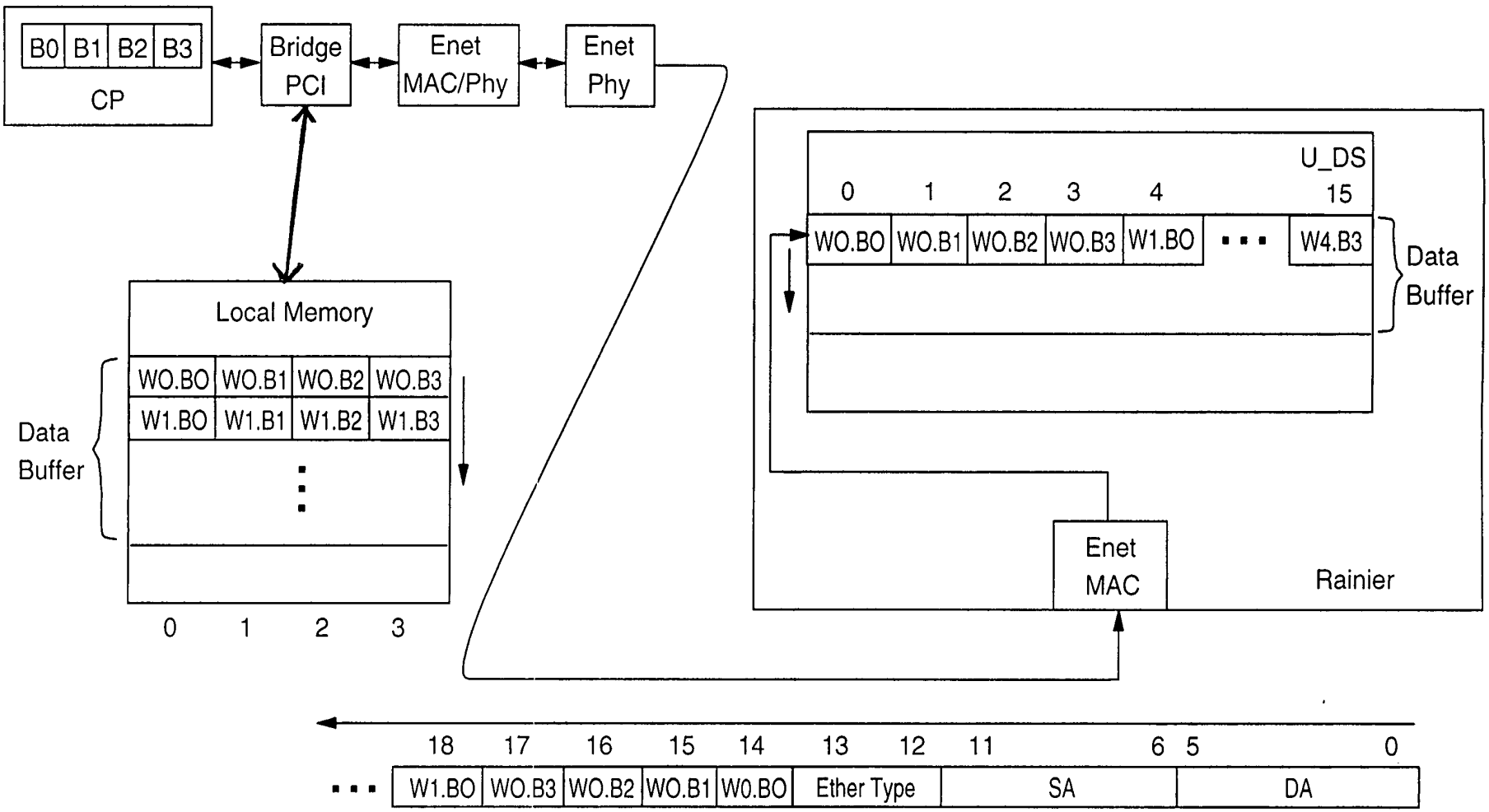
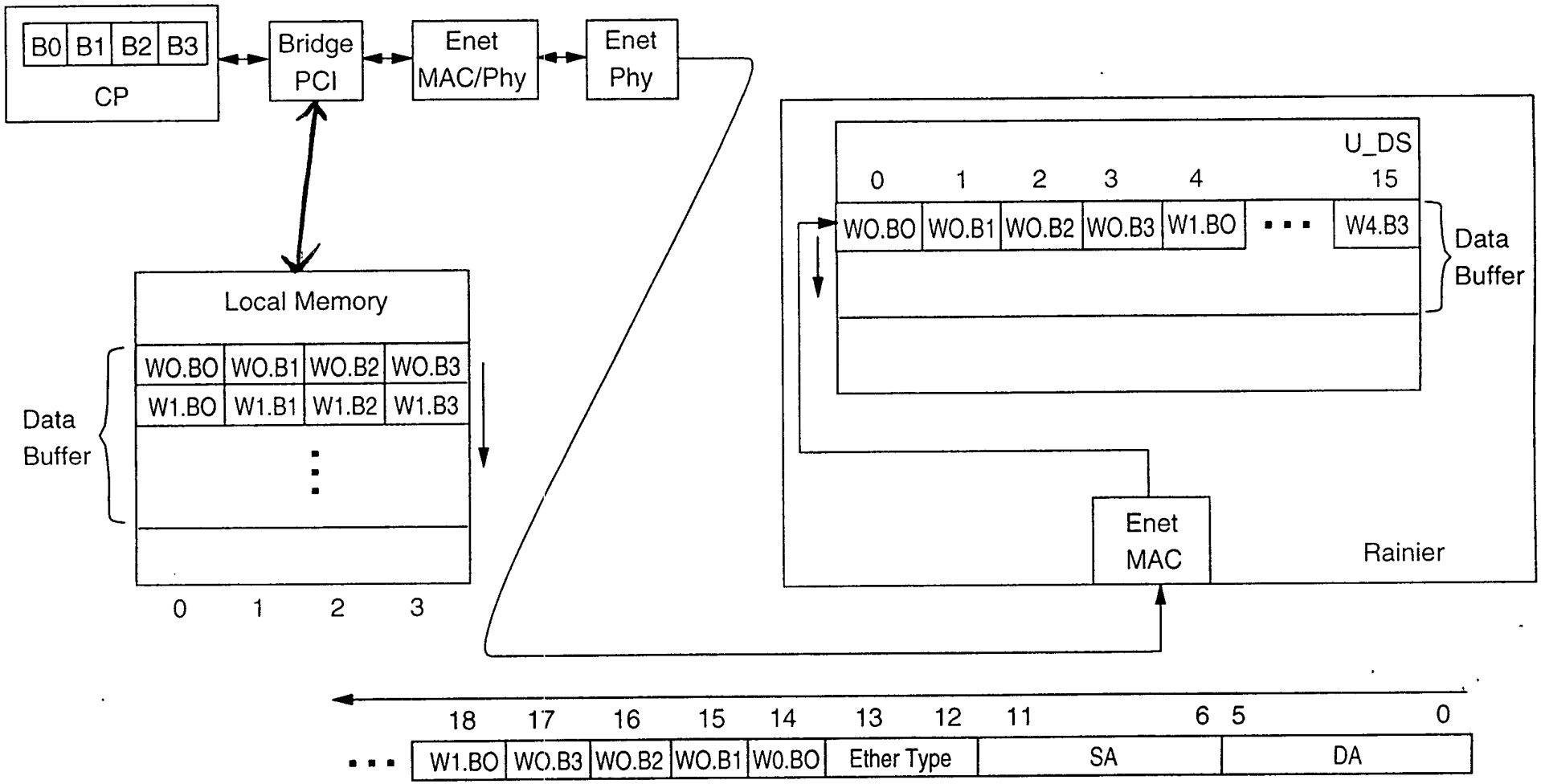


FIG. 3 Guided Traffic Data Flow (Ethernet Port)



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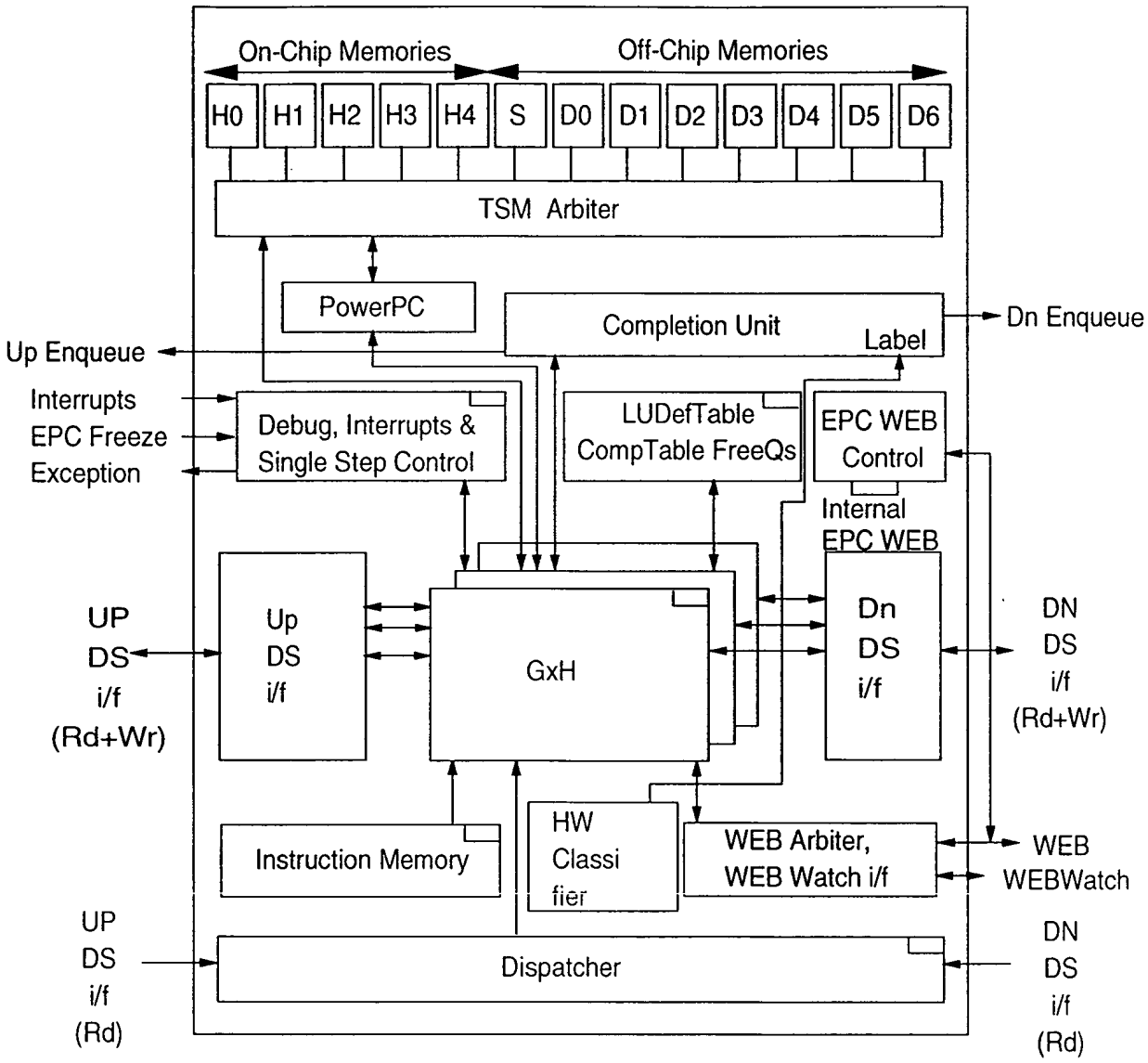

FIG. 12A BLOCK DIAGRAM OF THE EPC

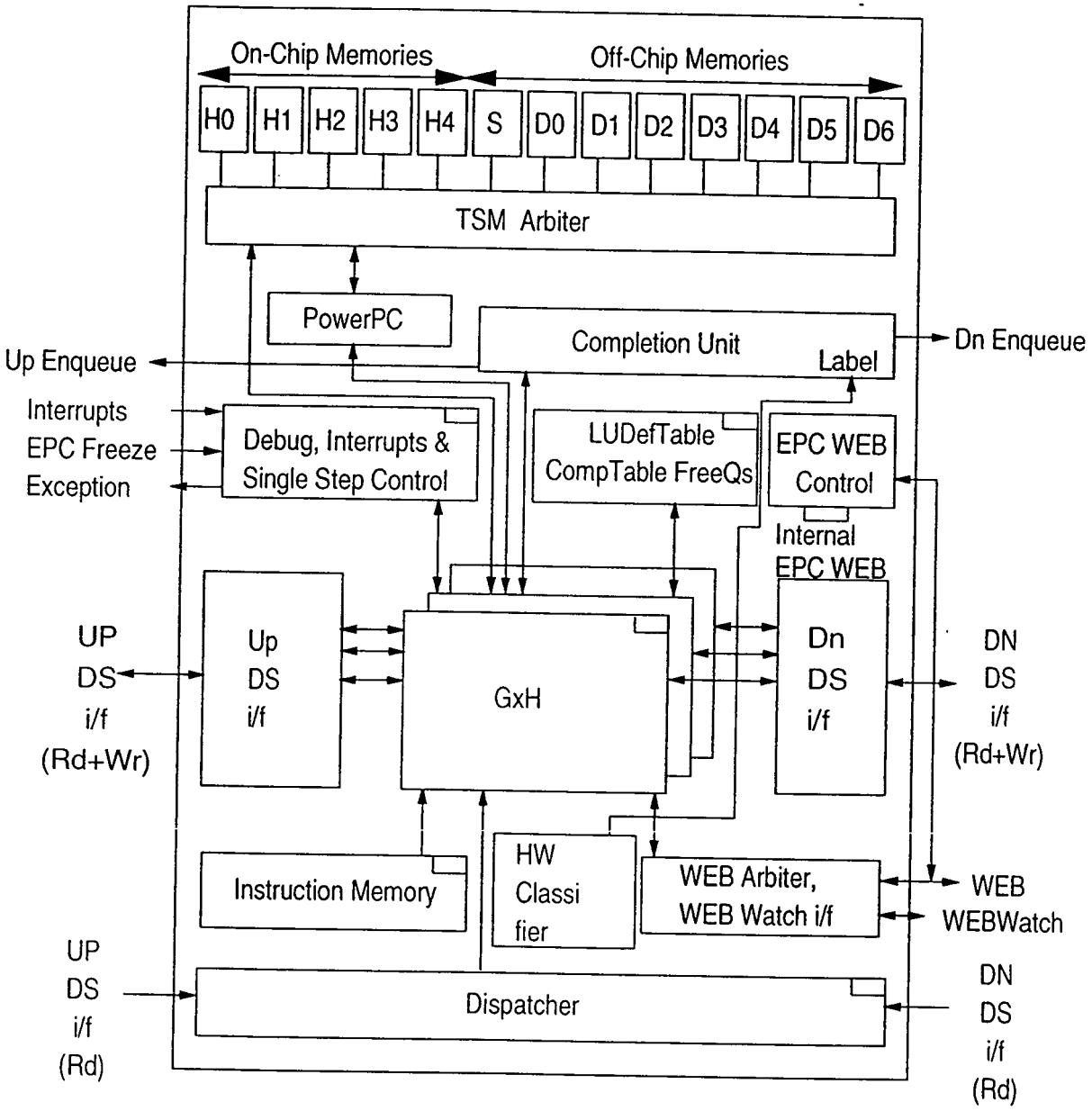

FIG. 12A BLOCK DIAGRAM OF THE EPC

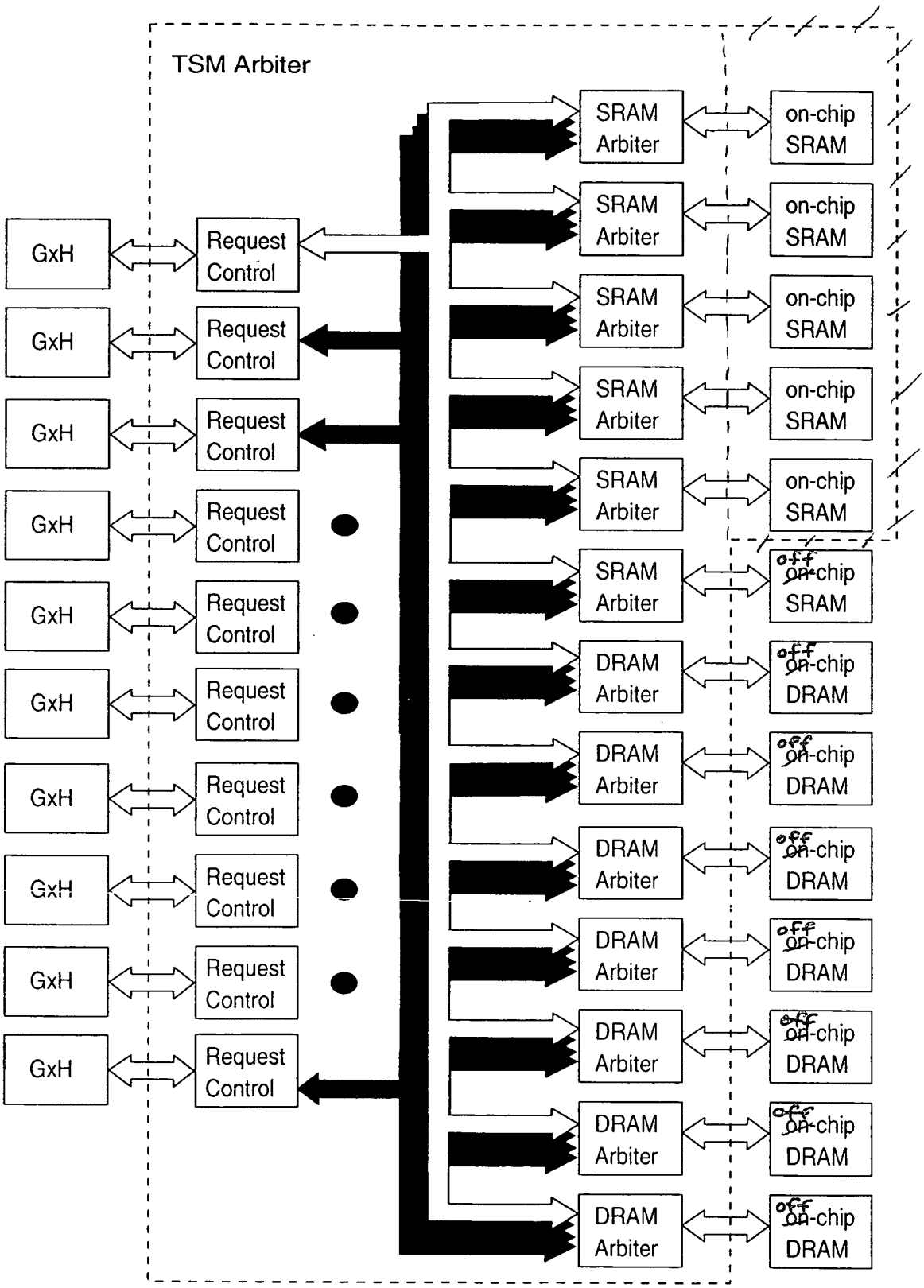

FIG. 13 (Memory Complex)

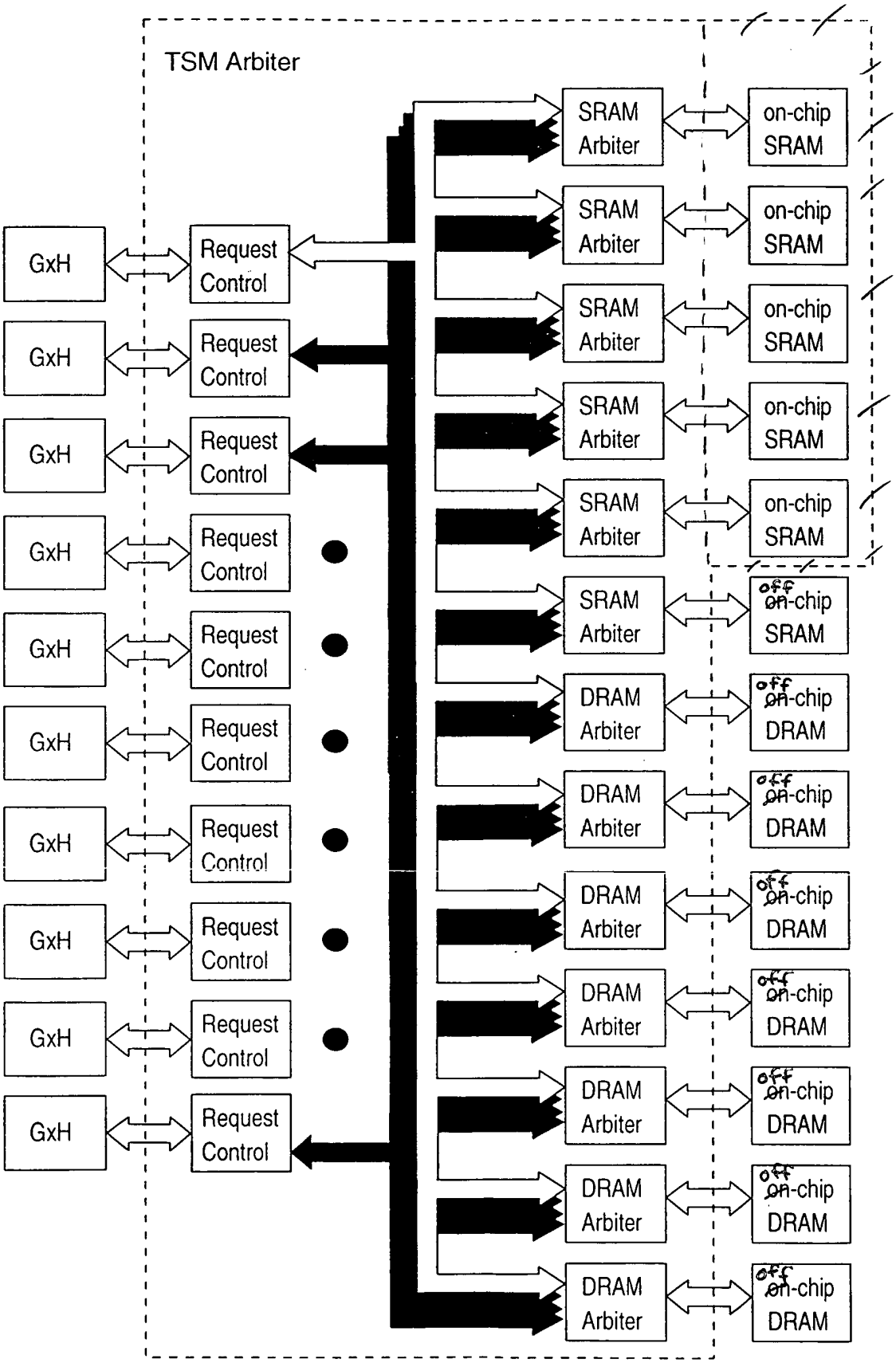

FIG. 13 (Memory Complex)